ABSTRACT OF THE DISCLOSURE

Semiconductor processing methods of forming transistors, semiconductor processing methods of forming dynamic random access memory circuitry, and related integrated circuitry are described. In one embodiment, active areas are formed over a substrate, with one of the active areas having a width of less than one micron, and with some of the active areas having different widths. A gate line is formed over the active areas to provide transistors having different threshold voltages. Preferably, the transistors are provided with different threshold voltages without using a separate channel implant for the transistors. In another embodiment, a plurality of shallow trench isolation regions are formed within a substrate and define a plurality of active areas having widths at least some of which being no greater than about one micron (or less), with some of the widths preferably being different. One or more gate lines may be coupled to the respective active areas to provide individual transistors, with the transistors corresponding to the active areas having the different widths having different threshold voltages. In another embodiment, two field effect transistors are fabricated having different threshold voltages without using a separate channel implant for one of the transistors versus the other.

Addendum

1. Semiconductor Processing Methods of Forming Transistors, Semiconductor Processing Methods of Forming Dynamic Random Access Memory Circuitry, and Related Integrated Circuitry